Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.170”**

**G**

**SOURCE**

**.230”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**GATE Bond Pad Size: .020 x .030”**

**Backside Potential: DRAIN**

**APPROVED BY: DK DIE SIZE .170” X .230” DATE: 3/8/23**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRF2804**

**DG 10.1.2**

#### Rev B, 7/1